I hereby certify that this correspondence is being deposited with the U. S. Postal Service on the date set forth below as First Class Mail in an envelope addressed to: Mail Stop MISSING PARTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date of Signature and Deposit: March 24, 2004

Attorney of Record

PATENT

Docket No. 121812.00005

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yang
Appl. No:	10/727,855
Filing Date:	December 4, 2003
Title:	DIGITAL RECEIVER
Group Art:	2631

CLAIM TO FOREIGN PRIORITY

Mail Stop MISSING PARTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Claim to foreign priority, based on Singapore Patent Application No. 200207436-7, filed December 5, 2002 is hereby lodged under 35 U.S.C. §119. A certified copy of the foreign priority document is submitted herewith.

No additional fee is believed to be due, but if any fee needs to be credited or charged, please charge Deposit Account No. 17-0055.

Respectfully submitted,

By:

Michael J. McGovern
Quarles and Brady LLP
411 East Wisconsin Ave.
Milwaukee, WI 53202
(414) 277-5725
Attorney of Record

QBMKE\5554829.1

REGISTRY OF PATENTS
SINGAPORE

This is to certify that the annexed is a true copy of application as filed for the following Singapore patent application.

Date of Filing	:	05 DECEMBER 2002
Application Number	:	200207436-7
Applicant(s) / Proprietor(s) of Patent	:	OKI TECHNO CENTRE (SINGAPORE) PTE LTD
Title of Invention	:	DIGITAL RECEIVER

SHARMAINE WU (Ms)
Assistant Registrar
for REGISTRAR OF PATENTS

G00001

PATENTS FORM 1
Patents Act
(Cap. 221)
Patents Rules
Rule 19

INTELLECTUAL PROPERTY OFFICE OF SINGAPORE

REQUEST FOR THE GRANT OF A PATENT UNDER SECTION 25

101101

* denotes mandatory fields

1. YOUR REFERENCE* SP5103

2. TITLE OF INVENTION* DIGITAL RECEIVER

3. DETAILS OF APPLICANT(S)* (see note 3)

Number of applicant(s): 1

(A) Name: Oki Techno Centre (Singapore) Pte Ltd

Address: 10 Collyer Quay, #19-08 Ocean Building
Singapore 049315

State:

Country: SG

[X] For corporate applicant

[ ] For individual applicant

State of incorporation:

State of residency:

Country of incorporation: SG

Country of residency:

[ ] For others (please specify in the box provided below)

(B) Name:

Address:

State:

Country:

200207436-7
05 DEC 2002

ACTION

☐ For corporate applicant

State of incorporation

Country of incorporation

☐ For individual applicant

State of residency

Country of residency

☐ For others (please specify in the box provided below)

(C) Name

Address

State

Country

☐ For corporate applicant

State of incorporation

Country of incorporation

☐ For individual applicant

State of residency

Country of residency

☐ For others (please specify in the box provided below)

☐ Further applicants are to be indicated on continuation sheet 1

---

4. DECLARATION OF PRIORITY (see note 5)

A. Country/country designated

File number

Filing Date DD MM YYYY

B. Country/country designated

File number

Filing Date DD MM YYYY

☐ Further details are to be indicated on continuation sheet 6

---

5. INVENTOR(S)* (see note 6)

A. The applicant(s) is/are the sole/joint inventor(s) Yes ☐ No X

200207436-7

05 DEC 2002

B. A statement on Patents Form 8 is/will be furnished Yes [X] No [ ]

6. CLAIMING AN EARLIER FILING DATE UNDER (see note 7)

[ ] section 20(3) [ ] section 26(6) [ ] section 47(4)

Patent application number [ ]

DD MM YYYY

Filing Date [ ]

Please mark with a cross in the relevant checkbox provided below
(Note: Only one checkbox may be crossed.)

[ ] Proceedings under rule 27(1)(a)

DD MM YYYY

Date on which the earlier application was amended [ ]

[ ] Proceedings under rule 27(1)(b)

7. SECTION 14(4)(C) REQUIREMENTS (see note 8)

Invention has been displayed at an international exhibition. Yes [ ] No [X]

8. SECTION 114 REQUIREMENTS (see note 9)

The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty.

Yes [ ] No [X]

9. CHECKLIST*

(A) The application consists of the following number of sheets

i.	Request	5	Sheets
ii.	Description	16	Sheets
iii.	Claim(s)	5	Sheets
iv.	Drawing(s)	5	Sheets
v.	Abstract (Note: The figure of the drawing, if any, should accompany the abstract)	1	Sheets
	Total number of sheets	32	Sheets

(B) The application as filed is accompanied by:

[ ] Priority document(s) [ ] Translation of priority document(s)

200207436-7
05 DEC 2002

x	Statement of inventorship & right to grant		International exhibition certificate

10. DETAILS OF AGENT (see notes 10, 11 and 12)

Name

Firm LLOYD WISE

11. ADDRESS FOR SERVICE IN SINGAPORE* (see note 10)

Block/Hse No. | Level No. | Unit No./PO Box

Street Name P.O BOX 636

Building Name TANJONG PAGAR POST OFFICE

Postal Code 910816

12. NAME, SIGNATURE AND DECLARATION (WHERE APPROPRIATE) OF APPLICANT OR AGENT* (see note 12)
(Note: Please cross the box below where appropriate.)

X I, the undersigned, do hereby declare that I have been duly authorised to act as representative, for the purposes of this application, on behalf of the applicant(s) named in paragraph 3 herein.

Name and Signature LLOYD WISE

DD MM YYYY
05 12 2002

Our Ref: SP5103

200207436-7
0 5 DEC 2002

NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the rest of the application. Please note that the filing fee should be furnished within the period prescribed.

2. The relevant checkboxes as indicated in bold should be marked with a cross where applicable.

3. Enter the name and address of each applicant in the spaces provided in paragraph 3.
Where the applicant is an individual
- Names of individuals should be indicated in full and the surname or family name should be underlined.
-The address of each individual should also be furnished in the space provided.
- The checkbox for "For individual applicant" should be marked with a cross.

   Where the applicant is a body corporate
- Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided.
- The address of the body corporate should also be furnished in the space provided.
- The checkbox for "For corporate applicant" should be marked with a cross.

   Where the applicant is a partnership
- The details of all partners must be provided. The name of each partner should be indicated in full and the surname or family name should be underlined.
- The address of each partner should also be furnished in the space provided.
- The checkbox for "For others" should be marked with a cross and the name and address of the partnership should be indicated in the box provided.

4. In the field for "Country", please refer to the standard list of country codes made available by the Registry of Patents and enter the country code corresponding to the country in question.

5. The declaration of priority in paragraph 4 should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under section 17 of the Patents Act] should be identified and the country should be entered in the space provided.

6. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph 5 should be completed by marking with a cross the 'YES' checkbox in the declaration (A) and the 'NO' checkbox in the alternative statement (B). Where this is not the case, the 'NO' checkbox in declaration (A) should be marked with a cross and a statement will be required to be filed on Patents Form 8.

7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified in paragraph 6 and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(a), they should also indicate the date on which the earlier application was amended.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' checkbox at paragraph 7 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' checkbox at paragraph 8 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross. Attention is also drawn to the Fourth Schedule of the Patents Rules.

10. Where an agent is appointed, the fields for "DETAILS OF AGENT" and "ADDRESS FOR SERVICE IN SINGAPORE" should be completed and they should be the same as those found in the corresponding Patents Form 41. In the event where no agent is appointed, the field for "ADDRESS FOR SERVICE IN SINGAPORE" should be completed, leaving the field for "DETAILS OF AGENT" blank.

11. In the event where an individual is appointed as an agent, the sub-field "Name" under "DETAILS OF AGENT" must be completed by entering the full name of the individual. The sub-field "Firm" may be left blank. In the event where a partnership/body corporate is appointed as an agent, the sub-field "Firm" under "DETAILS OF AGENT" must be completed by entering the name of the partnership/body corporate. The sub-field "Name" may be left blank.

12. Attention is drawn to sections 104 and 105 of the Patents Act, rules 90 and 105 of the Patents Rules, and the Patents (Patent Agents) Rules 2001.

13. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least 2 months after the application has been filed in Singapore, and unless no directions had been issued under section 33 by the Registrar or such directions have been revoked. Attention is drawn to sections 33 and 34 of the Patents Act.

14. If the space provided in the patents form is not enough, the additional information should be entered in the relevant continuation sheet. Please note that the continuation sheets need not be filed with the Registry of Patents if they are not used.

200207436-7
0 5 DEC 2002

0 5 DEC 2002

159159

G00002

200207436-7

DIGITAL RECEIVER

FIELD OF THE INVENTION

The present invention relates to a digital receiver suitable for use in a Burst-mode communication system.

BACKGROUND OF THE INVENTION

Low power consumption, cost-reduction, and compact size are some of the key features of a mobile/personal communication system such as GSM, DECT and Bluetooth based systems. Full integration is a very important way to reduce cost and size. The zero-IF receiver can be implemented in a highly integrated way. However, it suffers from dc offset, self-mixing, and mismatch between the different downconversion paths. The use of zero-IF is limited due to its poor performance. Although the conventional IF (heterodyne) receiver can achieve good performance, its implementation needs many off-chip components, which makes it vulnerable, expensive, and sensitive to external parasitic signals. Its power consumption is also increased. Accordingly, a need exists in the art to provide a digital receiver which can be implemented in a highly integrated way while still maintaining high quality signal reception.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, there is provided a digital receiver, comprising: a frequency converter arranged to convert a received signal into baseband signals; delay units arranged to delay the baseband signals to provide delayed signals; normalizing means arranged to truncate the baseband signals and the delayed signals to a predetermined length and provide

normalized signals; a demodulator arranged to demodulate the normalized signals and provide a demodulated signal; and frequency offset sensing means arranged to sense an envelope of the demodulated signal to provide an envelope signal.

Typically, the normalizing means is arranged to truncate the baseband signals and the delayed signals by: selecting from the baseband signals and the delayed signals one with the largest absolute value; determining a bit position of most significant bit of the selected signal; truncating each of the signals to the pre-determined length dependent upon the bit position.

Typically, the frequency offset sensing means comprises: means arranged to track the envelop of the demodulated signal to provide a tracking signal; and filter arranged to low pass filter the tracking signal to provide the envelope signal.

An advantage of the present invention is to provide a digital receiver suitable to be implemented in the form of an application specific integrated circuit (ASIC) with the specific design features of low power consumption and small size.

Another advantage of the present invention is to provide a simple normalization scheme to truncate a signal without introducing unacceptable distortion.

Still another advantage of the present invention to provide a method and apparatus arranged to estimate and compensate effects of the frequency offset between the transmitter and receiver in the system.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be discussed, by way of example, with reference to the accompanying drawings in which like reference characters identify correspondingly throughout and wherein:

Fig. 1 schematically illustrates a first embodiment of a digital receiver according to the present invention;

Fig. 2 schematically illustrates the structure of an analog front-end of the digital receiver shown in Fig. 1;

Fig. 3 shows an example of the operation of a normalizer of the digital receiver of Fig. 1;

Fig. 4 is a schematic block diagram illustrating the structure of a demodulator of the digital receiver shown in Fig. 1;

Fig. 5 is a schematic block diagram illustrating the structure of a filtering device of the digital receiver shown in Fig. 1;

Fig. 6 is a flow chart of the algorithm for computing the low frequency component caused by the frequency offset in the filtering device of Fig. 5;

Fig. 7 schematically illustrates a second embodiment of a digital receiver according to the present invention;

Fig. 8 is a schematic block diagram illustrating the structure of a demodulator of the digital receiver shown in Fig. 7;

Fig. 9 is a schematic block diagram illustrating the structure of a filtering device of the digital receiver shown in Fig. 7; and

Fig. 10 is a flow chart of the algorithm for computing the low frequency component caused by the frequency offset in the filtering device of Fig. 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

A first embodiment of a digital receiver for a burst-mode communication system is shown in Fig. 1. The receiver 1 includes an analogue front-end 100 arranged to convert a RF signal received from an antenna into a low IF signal; an AD converter 101 arranged to provide analogue-to-digital conversion of the output from the analogue front-end 100; a pair of mixers 102 and 103, coupled to the output of the AD converter 101, arranged to mix the AD converted signal with sine and cosine signals respectively to obtain two orthogonal components of the low IF signal, namely, I'_n and Q'_n; a pair of low pass filter (LPF) 104 and 105, coupled to the pair of mixers, arranged to filter high frequency contents of the two orthogonal components to obtain two baseband orthogonal components, namely, I_n and Q_n; a pair of delay units 106 and 107, coupled to the pair of LPF 104 and 105, arranged to delay the two baseband orthogonal components I_n and Q_n by a sampling period, T_S, to obtain two delayed components I_{n-1} and Q_{n-1}; a normalizer 108, coupled to the outputs of the pair of LPF 104 and 105, as well as the outputs of the pair of delay units 106 and 107, arranged to normalize the four components (i.e., I_n, Q_n, I_{n-1} and Q_{n-1}) by truncating them to pre-determined lengths of L bits, to yield four normalized signals, I''_n, I''_{n-1}, Q''_n and Q''_{n-1}; demodulator 109 arranged to demodulate the normalized signals from the normalizer 108; a filtering device 110 arranged to low frequency filter the demodulated signal x_n so as to obtain its average value dc_n; a decider 111 arranged to decide a tentative signal $\hat{b}_n$ according to the demodulated signal x_n

and the average value dc_n; and a symbol timing recovery 112 arranged to recover the symbol timing of the tentative signal $\hat{b}_n$.

Hereinafter, with reference to Figs. 2-6, the operations of the analog front-end 100, normalizer 108, demodulator 109, filtering device 110 will be explained.

Fig. 2 schematically illustrates the structure of the analog front-end 100 of the digital receiver 1 shown in Fig. 1. The analog front-end 100 includes a band-pass filter 200 arranged to filter the signal received from the antenna; a low noise amplifier 201, covering the whole bandwidth of the receiver 1, arranged to provide low noise amplification of the band-pass filtered signal from BPF 200 to suppress out-of block parts of the received signal; a voltage controlled oscillator 202 arranged to generate a local oscillating signal; a mixer 203 arranged to mix the amplified signal from LNA 201 with the local oscillating signal from VCO 202 to downconvert the frequency of the received signal into a low intermediate frequency (IF); a complex band-pass filter 204, centered at f_{IF}, arranged to band-pass filter the signal from the mixer to suppress its mirror signal; an AGC control circuit 205 arranged to detect the strength of the filtered signal from the complex band-pass filter 204 and control a gain of the following amplifier 206; an amplifier 206 arranged to amplify the filtered signal from the complex band-pass filter 204 under the gain-control of AGC 205.

The above-described analog front end 100 functions to convert the frequency of the received signal from the antenna from a radio frequency into a low intermediate frequency. A low intermediate frequency is an intermediate frequency lower than a conventional intermediate frequency. A low-IF receiver, like a zero-IF receiver, has a multi-path topology suitable for a highly integrated design to reduce cost and size. It uses an IF frequency of a few hundred kilohertz and is insensitive to parasitic baseband signals, such as dc offset and self-mixing

products. The low-IF receiver combines the advantages of both the conventional IF and the zero-IF receivers. It also has a high performance and is highly integrable. Moreover, due to use of the complex bandpass filter 204, following the analog front-end 100, only one AD converter is needed for analog-digital conversion of the low IF signal into a digital signal r_n at a fixed sampling frequency f_s. The output signal r_n from the AD converter is represented as:

$$r_n = A\cos\left[2\pi(f_{IF}+\Delta_f)nT_s+\Phi_n+\theta\right]+n_n, \qquad (1)$$

where, A is the amplitude of the digital signal, Δ_f is the frequency offset between the transmitter and receiver in the system, which is caused by the discrepancy between the oscillators at the transmitter and receiver or the Doppler effect, θ is the phase offset introduced by the VCO of the receiver, n_n and Φ_n are the nth samples of white Gaussian noise and the phase of GFSK modulated signal respectively.

The low IF signal from the AD 101 is further downconverted into a basedband signal by the pairs of mixers (102, 103) and low pass filters (104 and 105). In the mixers 102 and 103, the digital signals from AD 101 are mixed with sine and cosine signals, $\sin 2\pi f_{IF}t$ and $\cos 2\pi f_{IF}t$, respectively, to obtain two orthogonal components, I_n' and Q_n'. After filtering high frequency terms of the two orthogonal components by the pair of LPFs 104 and 105, two orthogonal baseband components (i.e., in-phase and quadrature base band components I_n and Q_n) are produced as follows:

$$\begin{aligned} I_n &= -A\sin\left[2\pi\Delta_f nT_s+\Phi(nT_s)+\theta\right] \\ Q_n &= A\cos\left[2\pi\Delta_f nT_s+\Phi(nT_s)+\theta\right] \end{aligned} \qquad (2)$$

If $f_s = 4f_{IF}$, then the above sine and cosine signals can be simplified as bit sequences 0,1,0,1 and 1,0,-1,0. This technique greatly simplifies the design for

the mixers, since the mixing of the digital signal from AD 101 with the two bit sequences needn't be implemented by multipliers.

At the receiver side, the amplitude of its output signal depends on the transmitted signal power, the propagation loss, the fading environment and the AGC. Therefore, the output from the digital receiver may have many bits and the valid signal range may vary due to the aforementioned factors. To minimize the logic size and power consumption of the receiver, before passing the four components, I_n, Q_n from the pair of LPFs and I_{n-1}, Q_{n-1} from the pair of delay units, to the demodulator 109 for further processing, a simple normalizer 108 is adopted to automatically truncate the lengths of these components from N bits to L bits (L<N). L is experimentally determined so that the truncation of signals will not degrade the performance of the receiving system.

Referring Fig. 3, an example of the operation of the normalizer 108 is discussed in detail. It is assumed that the lengths of the four components (I_n, I_{n-1}, Q_n, Q_{n-1}) input into the normalizer are N bits and the lengths of the outputs from the normalizer are L bits. The four components (I_n, I_{n-1}, Q_n, Q_{n-1}) are signed data. The normalization procedure comprises the following steps:

- Find the input with the maximum absolute value from the four input components. In this example, the input with the maximum absolute value is I_{n-1}.

- Determine the bit position of the most significant bit of the input component having the maximum absolute value. Most significant bit means a bit which makes the largest contribution to the absolute value of binary data. If the binary data is a signed data, the most significant bit is the first bit whose value is different from that of its sign bit. For I_{n-1}, since the value of its sign bit is '0', most significant bit thereof shall be the first bit whose value is '1'. From Fig. 3, it can be

seen that the bit position of most significant bit of I_{n-1} is N-2, and is recorded as i (i=N-2).

• Truncate each of the inputs to a pre-determined length of L bits. In this example, since the four inputs are signed data, their sign bits remain in their truncated signals. More particularly, the four inputs are truncated by selecting L-1 bits of each input starting from the bit position determined in the above step, i.e., L-1 bits between the i th and (i-L-2) th bits, and then adding a sign bit of each of the inputs. In the example shown in Fig. 3, the four inputs are truncated by selecting L-1 bits from the (N-2) th bit to the (N-L-4) th bit (i.e., the fifth bit) and adding the sign bit of each input (i.e., sign bits 0, 0, 1 and 1) as a first bit of each truncated signal. The four truncated signals I_n, I_{n-1}, Q_n, Q_{n-1} with the pre-determined length of L bits are shown on the right side of Fig. 3.

The truncated data $I_n^{\prime r}, I_{n-1}^{\prime r}, Q_n^{\prime r}, Q_{n-1}^{\prime r}$ is inputted to the demodulator 109 as depicted in Fig.4. The demodulator 109 comprises a pair of multipliers 400 and 401 to cross multiple the four truncated inputs by multiplying $I_n^{\prime r}$ by $Q_{n-1}^{\prime r}$ and $Q_n^{\prime r}$ by $I_{n-1}^{\prime r}$. The demodulator 109 also includes an adder 402 arranged to add the outputs from the multipliers. After summing by the adder, The demodulator output is:

$$x_n = Q_n^{\prime r} I_{n-1}^{\prime r} - Q_{n-1}^{\prime r} I_n^{\prime r} = A^2 \sin\left(2\pi \Delta_f T_s + \Delta\Phi\right). \tag{3}$$

where, $T_s = \frac{T_b}{K}$ is the sampling duration, $\Delta\Phi = \Phi(nT_s) - \Phi((n-1)T_s)$ represents the phase difference during a sampling period.

The presence of frequency offset, Δ_f, degrades the overall system performance. Under ideal conditions, the frequency offset $\Delta_f = 0$, the expectation value of the demodulator output is $A^2 \sin\Delta\Phi$. However, in practice,

the frequency offset Δ_f is always non-zero. From Eqn(3), it can be seen that the demodulator output x_n has been distorted by the frequency offset.

When $2\pi\Delta_f T_s$ is small, the expression of Eqn(3) can be approximated by:

$$x_n \approx A^2(2\pi\Delta_f \cos\Delta\Phi + \sin\Delta\Phi) \qquad (4)$$

The expectation value of x_n in Eqn(4) is:

$$E[x_n] = A^2(2\pi\Delta_f E[\cos\Delta\Phi] + E[\sin\Delta\Phi]) \qquad (5)$$

Under the assumption of equally distributed input data, it can be seen that E[sin $\Delta\Phi$] =0. From Eqn(5), the frequency offset produces a low frequency signal $A^2\, 2\pi\Delta_f \cos\Delta\Phi$ at the output of the demodulator 109. A reference signal for the following decider 111 needs to be non-zero to compensate the frequency offset. A filtering device 110, a block diagram of the structure and a flow chart of the operation of which are respectively depicted in Figs. 5 and 6, provides a mechanism for tracking and filtering the low frequency signal caused by the frequency offset.

In the prior art, such as US Patent 5448594, entitled "One-bit Differential Demodulator", a low pass filter is designed to track the low frequency signal $A^2 2\pi\Delta_f \cos\Delta\Phi$ directly. The disadvantage of this method is that if the bandwidth of the filter is excessive, the resultant output will contain too much high frequency content, which endangers the proper operation of the differential detector. If the bandwidth of the filter is insufficient, a long time is needed to capture the burst data. Instead of tracking the low frequency component directly, in the present invention,, the envelope of the demodulator output x_n is tracked and low-pass filtered to obtain the low frequency component. As the envelope of the demodulated signal tends to be more stable than the demodulated signal itself, a

LPF with a much wider bandwidth can be employed to give a fast tracking without introducing too much disturbance. A separate feature which allows a further improvement in performance, i.e., capture of the data in a shorter time while keeping a good BER performance simultaneously, is the use of an adaptive low pass filter. During the beginning of the data reception, the filter can be allowed to begin operation at a wider bandwidth. This is useful in terms of capturing the burst data quickly. As more data is received, the bandwidth of the filter is reduced gradually in order to suppress the high frequency components.

The filtering device of the present invention is composed of three main functional blocks: a tracker 500, an adaptive IIR filter 501 and a coefficient of Adaptive IIR filter generator 502. Referring Fig. 6, at the beginning of the loop, the parameters α, Max, Min and dc are preset to an appropriate value (e.g., zero), in which parameter α is a coefficient of the IIR filter 501, Max and Min are respectively the values of positive and negative peaks of the envelope of the demodulator output x_n, and dc is the output of the IIR filter 501, i.e., low frequency component of the envelope of the demodulator output x_n. The values of the positive and negative peaks Max, Min of the input signal x_n are updated by using tracker 500 based on the following rules:

- if $x_n < x_{n-1} > x_{n-2}$ and $x_{n-1} > Min + threshold$ and $x_{n-1} < MAX$,
  And if $x_{n-1} > Max$ or $x_{n-1} > dc_{n-1}$, then $Max = x_{n-1}$
- if $x_n > x_{n-1} < x_{n-2}$ and $x_{n-1} < Max - threshold$ and $x_{n-1} > -MAX$,
  And if $x_{n-1} < Min$ or $x_{n-1} < dc_{n-1}$, then $Min = x_{n-1}$

where, x_n, x_{n-1}, x_{n-2} are samples of the demodulator output at time n, time n-1 and time n-2, respectively. The parameter "threshold" is a user-defined constant reflecting the smallest gap between the positive and negative peaks. The parameter "MAX" is also a user-defined constant, wherein the tracked positive and negative peaks are confined within the range (-MAX, MAX). Moreover,

"threshod" and "MAX" are proportional to the sampling duration, the modulation index being employed, as well as the amplitude of the input signal. Coefficient of adaptive IIR filter generator 502 adjusts the coefficient α_n of the IIR filter 501 at time n to reduce the bandwidth of the adaptive IIR filter. The coefficient α_n at time n is reduced as a function of time, for example, $\alpha_n = \frac{31}{32}\alpha_{n-1} + \frac{1}{32} * \frac{1}{256}$. The maximum and the minimum values Max, Min and the parameter α_n are used as the inputs to the adaptive IIR filter 501 for the calculation of the low frequency component of the envelope of the demodulator output x_n according to the following equation

$$dc_n = (1-\alpha_n)dc_{n-1} + \frac{\alpha_n}{2}(Max + Min) \tag{6}$$

where, dc_n is the low frequency component of the envelope of the signal x_n at time n,

dc_{n-1} is the low frequency component of the envelope of the signal x_{n-1} at time n-1, α_n is the filter coefficient at time n.

The above process is repeated as long as the communication device is in operation. The signal dc_n is used as an input to a decider 111 of Fig. 1 as a reference signal. The decider 111 makes a hard decision or soft decision to yield a tentative signal $\hat{b}_n$. For a hard decision, the decider 111 can be a comparator which makes decision according to the following rule:

$$\hat{b}_n = \begin{cases} 1, & x_n > dc_n \\ 0, & x_n \le dc_n \end{cases}$$

However, for a soft decision, the decider 111 can be a subtractor, which subtracts the output of the filtering device, dc_n, from that of the demodulator 109, x_n, and a comparator, which makes decision according to the following rule:

$$\hat{b}_n = \begin{cases} 1, & x_n - dc_n > 0 \\ 0, & x_n - dc_n \le 0 \end{cases}$$

Based on the filtering device, the effect of frequency offset can be estimated without using a frequency detector or a complex feedback loop. The symbol timing of the tentative signals $\hat{b}_n$ is recovered by the symbol timing recovery unit 112. Since all the values after the AD converter are fixed-point data, all calculations can be implemented by simple logical operations such as shifting, addition, subtraction, XOR and so on. At the same time, the low-IF topology can be implemented with a high degree of integration and a high performance.

With reference to Figs. 7-10, a second embodiment of a digital receiver of the present invention will be explained.

Referring first to Fig. 7, a digital receiver 2 of the second embodiment includes an analogue front-end 100, an AD converter 101, a pair of mixers 102 and 103, a pair of LPFs 104 and 105, a pair of delay units 106 and 107, a normalizer 108, a demodulator 700, a filtering device 701, a decider 111, and a symbol timing recovery 112. It can be seen that the differences between the digital receiver 1 of Fig. 1 and the digital receiver 2 of Fig. 7 lie in the structures of their demodulators and their filtering devices.

Fig.8 is a schematic block diagram illustrating the structure of the demodulator 700 of the digital receiver 2 shown in Fig. 7. Comparing this demodulator 700 with the demodulator 109 of the digital receiver 1, the demodulator 700 of the receiver 2 further comprises means arranged to normalize the sum from the adder 402 to its signal power, including a pair of multipliers 800 and 801 arranged to self-multiply the two component I_n and Q_n, an adder 802 arranged to sum the outputs from the pair of multipliers, and a divider 803 arranged to divide the sum ($Q_n^{\prime\prime r} I_{n-1}^{\prime\prime r}$-$Q_n^{\prime\prime r} I_n^{\prime\prime r}$) from the adder 402 with the sum $\left(c_n^{'} = \left(I_n^{\prime\prime r}\right)^2 + \left(Q_n^{\prime\prime r}\right)^2\right)$ from the adder 802, yielding:

$$x_n = \frac{Q_n^{\prime r} I_{n-1}^{\prime r} - Q_{n-1}^{\prime r} I_n^{\prime r}}{(I_n^{\prime r})^2 + (Q_n^{\prime r})^2} = \sin(2\pi\Delta_f T_S + \Delta\Phi) \quad (7)$$

The sine of the change in phase of the received signal r(t) is obtained and is independent of the signal power. When $2\pi\Delta_f T_s$ is small, the expression of Eqn(7) can be approximated by:

$$x_n \approx 2\pi\Delta_f \cos\Delta\Phi + \sin\Delta\Phi \quad (8)$$

The expectation value of x_n in Eqn(8) yields:

$$E[x_n] = 2\pi\Delta_f E[\cos\Delta\Phi] + E[\sin\Delta\Phi] \quad (9)$$

For the reason given in the first embodiment, $E[\sin\Delta\Phi] = 0$. From Eqn(9), the frequency offset produces a low frequency signal $2\pi\Delta_f \cos\Delta\Phi$ at the output of the demodulator 700. The reference signal for the decider 111 is non-zero due to the frequency offset. A filtering device 701 is added in Fig.7 to adaptively track the low frequency signal $2\pi\Delta_f \cos\Delta\Phi$, which is used as the reference signal for the following decider 111. The detailed structure of the filtering device 701 is shown in Fig. 9. The difference between the filtering devices of Fig. 5 and 9 is that the filtering device 701 further comprises a reset signal generator 900 which is used to detect the start of data transmission and generate a reset signal to initiate the tracker 500, the adaptive IIR filter 501, and the coefficient of adaptive IIR filter generator 502, because in order to allow the receiver to operate properly in a burst mode communication system, it is important to determine when the burst data transmission starts. The inputs to the demodulator 700 are truncated signals, which makes the sum $c_n^{'}$ unable to accurately represent the signal power of the received signal. To correct this problem, before detecting the start of the burst data transmission, the reset signal generator 701 eliminates the effect of the normalizer on the signal power $c_n^{'}$ by shifting it according to the bit position i

from the normalizer 108. In this embodiment, the reset signal generator 900 right-shifts the signal power $c_n^{'}$ with 2(N-i-1) bits. It is apparent to an ordinary person skilled in the art that other methods can be applied to eliminate the effect of the normalization, which falls within the protective scope claimed by this application. The reset signal generator 900 further includes a simple LPF filter which is used to calculate the average value of the de-normalized signal, namely, the signal power c_n.

Fig. 10 shows the flow chart of the operation of the filtering device 701 of Fig. 9. Prior to the start of data transmission, the parameters α, Max, Min, dc and d should be reset to the pre-defined initialization values, in which parameter d is the output of the simple LPF filter of the reset signal generator 900. Then, the signal power $c_n^{'}$ from the demodulator 700 is de-normalized according to the bit position from the normalizer 108 and low-pass filtered by the reset signal generator 900 with the form $d_n = \sigma d_{n-1} + (1-\sigma)c_n$, where σ is a constant in the range of (0,1), to obtain an average value of the signal power c_n. The average value d_n of the signal power c_n is compared with its previous value d_{n-1} at the symbol rate to determine the start of the data transmission. In this embodiment, the average value d_n is compared with its weighted previous values γd_{n-kl}, in which γ represents a weighting factor of d_{n-kl}, K is the oversampling factor which is defined in Eqn.(3) and l is an integer (l=1,2,3...).

Then, the positive and negative peaks of the demodulator output x_n are tracked by tracker 500 based on the following rules:

- if $x_n < x_{n-1} > x_{n-2}$ and $x_{n-1} > Min + threshold$ and $x_{n-1} < MAX$,

  And if $x_{n-1} > Max$ or $x_{n-1} > dc_{n-1}$, then $Max = x_{n-1}$
- if $x_n > x_{n-1} < x_{n-2}$ and $x_{n-1} < Max - threshold$ and $x_{n-1} > -MAX$,

And if $x_{n-1} < Min$ or $x_{n-1} < dc_{n-1}$, then $Min = x_{n-1}$

Since the amplitude of the input signal to the demodulator 700 of Fig. 8 is normalized, the two pre-determined constants "threshold" and "MAX" are only proportional to the sampling duration, the modulation index being employed. The maximum and the minimum values Max, Min are used as the inputs to the adaptive IIR filter 501 for the calculation of the low frequency component according to the following equation

$$dc_n = (1-\alpha_n)dc_{n-1} + \frac{\alpha_n}{2}(Max + Min) \qquad (10)$$

The bandwidth of the adaptive IIR filter is reduced gradually by adjusting the coefficient α_n in the coefficient of adaptive IIR filter generator 502. The coefficient α_n is reduced as a function of time, for example, $\alpha_n = \frac{31}{32}\alpha_{n-1} + \frac{1}{32} * \frac{1}{256}$. The above process is repeated as long as the communication device is in operation. The signal dc_n is used as an input to a decider 111 of Fig. 7 as a reference signal. The decider 111 makes a hard decision or soft decision to yield a tentative signal $\hat{b}_n$. For a hard decision, the decider 111 can be a comparator which makes decision according to the following rule:

$$\hat{b}_n = \begin{cases} 1, & x_n > dc_n \\ 0, & x_n \le dc_n \end{cases}$$

However, for a soft decision, the decider 111 can be a subtractor, which subtracts the output of the filtering device, dc_n, from that of the demodulator 109,

$$\hat{b}_n = \begin{cases} 1, & x_n - dc_n > 0 \\ 0, & x_n - dc_n \le 0 \end{cases}$$

x_n, and a comparator, which makes decision according to the following rule:

Based on the filter device, the effect of frequency offset can be estimated without using frequency detector and complex feedback loop. The symbol timing of the tentative signals $\hat{b}_n$ is recovered by the symbol timing recovery unit 112.

In conclusion, a single-chip digital receiver for a burst mode communication system has been disclosed. The digital receiver of the present invention is suitable for implementation as an ASIC and is insensitive to frequency offset. The invention should not be restricted to the present form. For example, although in the disclosure of the present invention the decider is shown to directly follow the filtering device, it can be modified to follow other elements, such as a phase offset compensator which is arranged to compensate the phase offset existing in the signals output from the filtering device. Numerous modifications, changes, variations, substitutions and equivalents will occur to those skills in the art without departing from the spirit and scope of the present invention as defined by the following claims:

CLAIMS:

1. A digital receiver, comprising:

a frequency converter arranged to convert a received signal into baseband signals;

delay units arranged to delay the baseband signals to provide delayed signals;

normalizing means arranged to truncate the baseband signals and the delayed signals to a predetermined length and provide normalized signals;

a demodulator arranged to demodulate the normalized signals and provide a demodulated signal; and

frequency offset sensing means arranged to sense an envelope of the demodulated signal to provide an offset signal indicative of a frequency offset of the received signal.

2. A digital receiver according to claim 1, wherein the normalizing means is arranged to truncate the baseband signals and the delayed signals by:

finding a signal with the largest absolute value among the baseband signals and the delayed signals;

determining a bit position of most significant bit of the signal; and

truncating each of the baseband signals and the delayed signals to the pre-determined length dependent upon the bit position.

3. A digital receiver according to claim 2, wherein the baseband signals and the delayed signals are signed signals.

4. A digital receiver according to claim 3, wherein each of the normalized signals include a sign bit of each of the baseband signals and the delayed signals.

5. A digital receiver according to claims 2-4, wherein the pre-determined length is so determined that the normalized signals do not degrade the performance of the receiver.

6. A digital receiver according to any one of the preceding claims, wherein the frequency offset sensing means comprises:

means arranged to track the envelope of the demodulated signal to provide an envelope signal; and

filter arranged to low pass filter the envelope signal to provide the offset signal.

7. A digital receiver according to claim 6, wherein the filter is an adaptive IIR filter.

8. A digital receiver according to claims 6 or 7, wherein the sensing means further comprises a filter coefficient generator arranged to generate and adjust the coefficient of the filter.

9. A digital receiver according to claim 8, wherein the filter coefficient generator reduces the filter coefficient as a function of time.

10. A digital receiver according to claim 9, wherein the filter coefficient generator adjusts the filter coefficient according to the following:

$$\alpha_n = \frac{31}{32}\alpha_{n-1} + \frac{1}{32} * \frac{1}{256},$$

wherein α_n is the filter coefficient at time n, α_{n-1} is the filter coefficient at time n-1.

11. A digital receiver according to any one of the preceding claims, wherein the demodulator further comprises a power normalizing means arranged to

generate a power signal from the normalized signals and provide a normalized demodulated signal to the sensing means.

12. A digital receiver according to claim 11, wherein the sensing means further comprises:

a reset signal generator for detecting the start of input data transmission and reset the sensing means.

13. A digital receiver according to claim 12, wherein the reset signal generator is arranged to detect the power signal to detect the start of transmission.

14. A digital receiver according to claim 12, wherein the reset signal generator further de-normalize the power signal dependent upon the bit position from the normalizing means.

15. A digital receiver according to any one of the preceding claims, wherein the frequency converter comprises:

an analogue front-end arranged to convert a frequency of the received signal from a radio frequency into a low intermediate frequency to provide a low intermediate frequency signal.

16. A digital receiver according to claim 15, wherein the frequency converter further comprises:

an analogue-digital converter arranged to analogue-to-digital convert the low intermediate frequency signal to provide a digital signal;

mixers arranged to respectively mix the digital signal respectively with sine and cosine signals to obtain two orthogonal components; and

filters arranged to filter high frequency parts of the two orthogonal components to obtain the baseband signals.

17. A digital receiver according to any one of the preceding claims, further comprising:

deciding means arranged to decide a tentative signal from the demodulated signal and the offset signal.

18. A digital receiver according to claim 17, wherein the deciding means comprises a comparator arranged to compare the demodulated signal with the offset signal to provide the tentative signal.

19. A digital receiver according to claim 17, wherein the deciding means comprises:

a subtractor arranged to subtract the offset signal from the demodulated signal and provide a difference signal; and

a comparator arranged to compare the difference signal with zero to provide the tentative signal.

20. A digital receiver according to claims 17-19, further comprising a symbol timing recovery arranged to a symbol timing of the tentative signal.

21. A digital receiver according to any one of the preceding claims, wherein the sensing means is arranged to track the envelope of the demodulated signal by making the following determinations:

if $x_n < x_{n-1} > x_{n-2}$ and $x_{n-1} > Min + threshold$ and $x_{n-1} < MAX$,

And if $x_{n-1} > Max$ or $x_{n-1} > dc_{n-1}$, then $Max = x_{n-1}$

if $x_n > x_{n-1} < x_{n-2}$ and $x_{n-1} < Max - threshold$ and $x_{n-1} > -MAX$,

And if $x_{n-1} < Min$ or $x_{n-1} < dc_{n-1}$, then $Min = x_{n-1}$

where, x_n, x_{n-1}, x_{n-2} are samples at time n, at time n-1 and at time n-2 of the first input signal, respectively, dc_{n-1} is low frequency component of the envelope of the demodulated signal at time n-1, Max and Min are the envelope signal

which represent negative and positive peaks of the envelope of the demodulated signal, and threshold and MAX are preset constants.

22. A digital receiver according to claim 12, wherein the threshold and MAX are proportional to a sampling duration, a modulation index or amplitude of the demodulated signal.

23. A digital receiver according to claim 12 or claim 13, wherein the filter is arranged to calculate the frequency component of the envelope signal of the form:

$$dc_n = (1-\alpha_n)dc_{n-1} + \frac{\alpha_n}{2}(Max + Min)$$

where, dc_n is a frequency component of the envelope signal at time n, dc_{n-1} is the frequency component of the envelope signal at time n-1, α_n is the filter coefficient at time n.

24. A digital receiver, comprising:

a frequency converter arranged to convert a received signal into baseband signals;

delay units arranged to delay the baseband signals to provide delayed signals;

normalizing means arranged to truncate the baseband signals and the delayed signals to a predetermined length and provide normalized signals;

a demodulator arranged to demodulate the normalized signals and provide a demodulated signal; and

a filter arranged to filter the demodulated signal to provide a filtered signal and wherein the filter is arranged to have a bandwidth which decreases as a function of time.

ABSTRACT

DIGITAL RECEIVER

A digital receiver, comprising: a frequency converter (100, 101, 102, 103, 104, 105) arranged to convert a received signal into baseband signals; delay units (106, 107) arranged to delay the baseband signals to provide delayed signals; normalizing means (108) arranged to truncate the baseband signals and the delayed signals to a predetermined length and provide normalized signals; a demodulator (109) arranged to demodulate the normalized signals and provide a demodulated signal; and frequency offset sensing means (110) arranged to sense an envelope of the demodulated signal to provide an offset signal indicative of a frequency offset of the received signal.

FIG. 1

163163

G00002

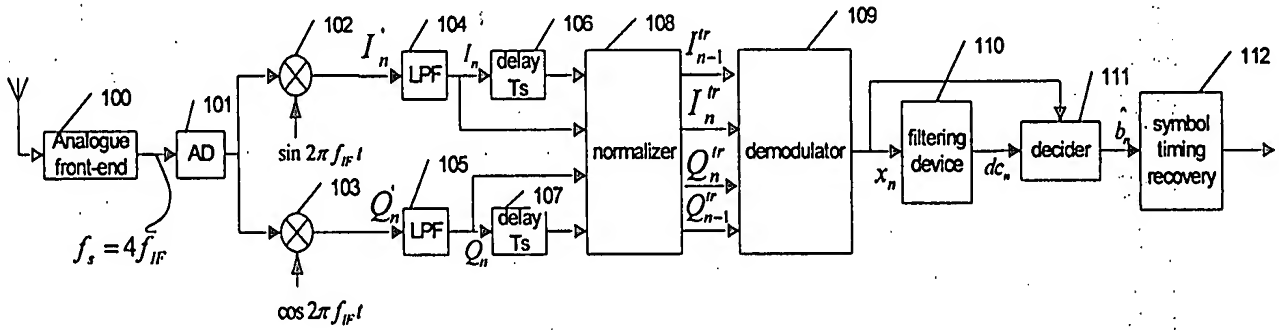

FIGURE 1

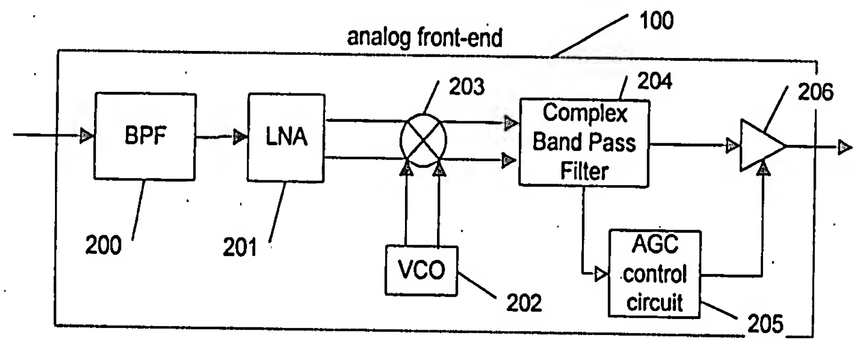

FIG. 2

bit position	N (sign bit)	N-1	N-2	N-3	...	6	5	4	3	2	1
I_n	0	0	0	1	...	1	0	0	1	0	0
I_{n-1}	0	0	1	0	...	1	0	1	0	0	1
Q_n	1	1	1	1	...	0	1	0	1	0	1
Q_{n-1}	1	1	1	1	...	1	0	1	0	1	0

L-1 Bits (bit positions N-2 to 5)

	sign bit					
I_n^{lr}	0	0	1	...	1	0
I_{n-1}^{lr}	0	1	0	...	1	0
Q_n^{lr}	1	1	1	...	0	1
Q_{n-1}^{lr}	1	1	1	...	1	0

L-1 Bits (the five bits after the sign bit)

I_{n-1} *has the* max*imum absolute value among* $I_{n-1}, I_n, Q_n, Q_{n-1}$

$i = N - 2$

FIG. 3

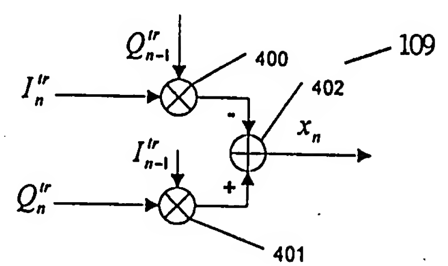

FIG. 4

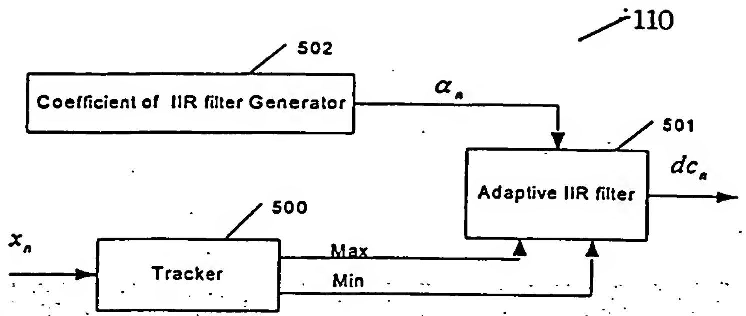
110
502
Coefficient of IIR filter Generator
α_n
501
Adaptive IIR filter
dc_n
500
x_n
Tracker
Max
Min

FIG. 5

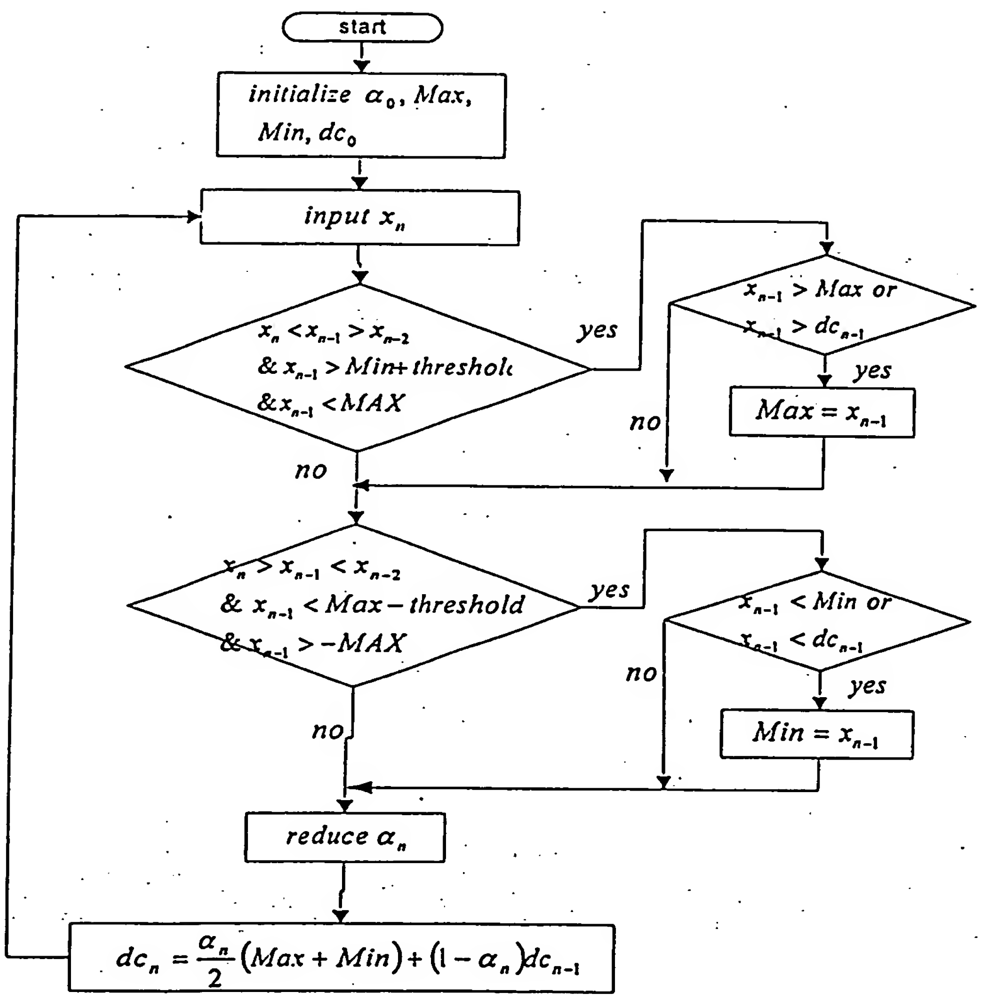
start
initialize α_0, Max, Min, dc_0
input x_n
$x_n < x_{n-1} > x_{n-2}$ & $x_{n-1} > Min + threshold$ & $x_{n-1} < MAX$
yes
no
$x_{n-1} > Max$ or $x_{n-1} > dc_{n-1}$
yes
no
$Max = x_{n-1}$
$x_n > x_{n-1} < x_{n-2}$ & $x_{n-1} < Max - threshold$ & $x_{n-1} > -MAX$
yes
no
$x_{n-1} < Min$ or $x_{n-1} < dc_{n-1}$
yes
no
$Min = x_{n-1}$
reduce α_n
$dc_n = \frac{\alpha_n}{2}(Max + Min) + (1 - \alpha_n)dc_{n-1}$

FIG. 6

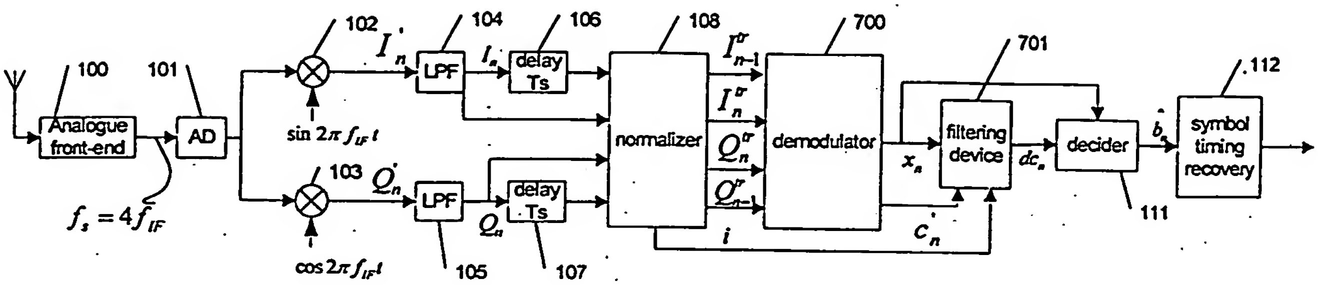

FIGURE 7

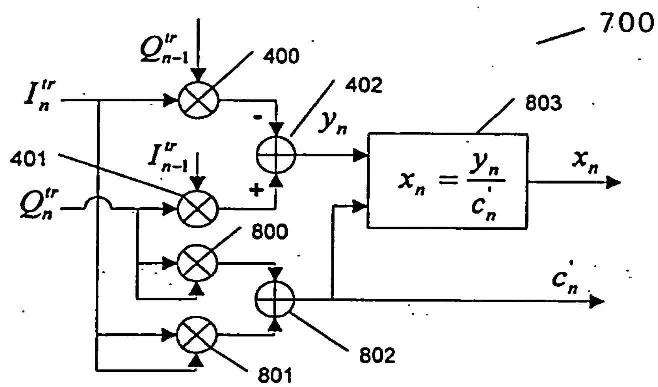

FIG. 8

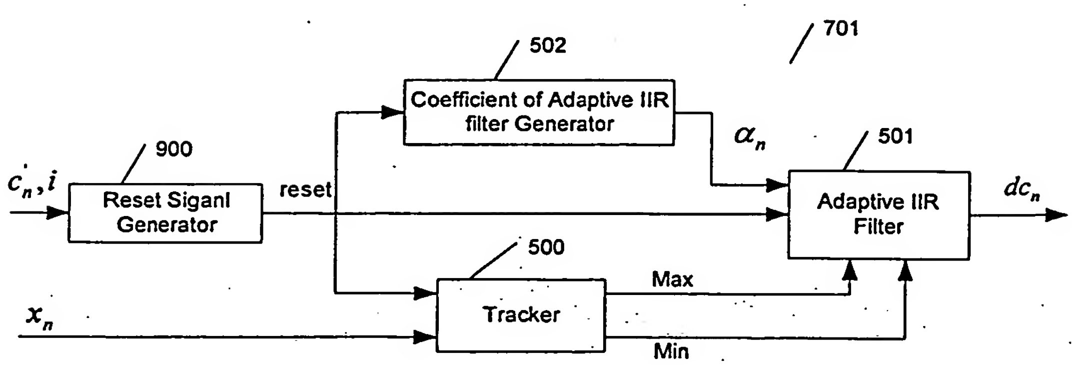

FIG. 9

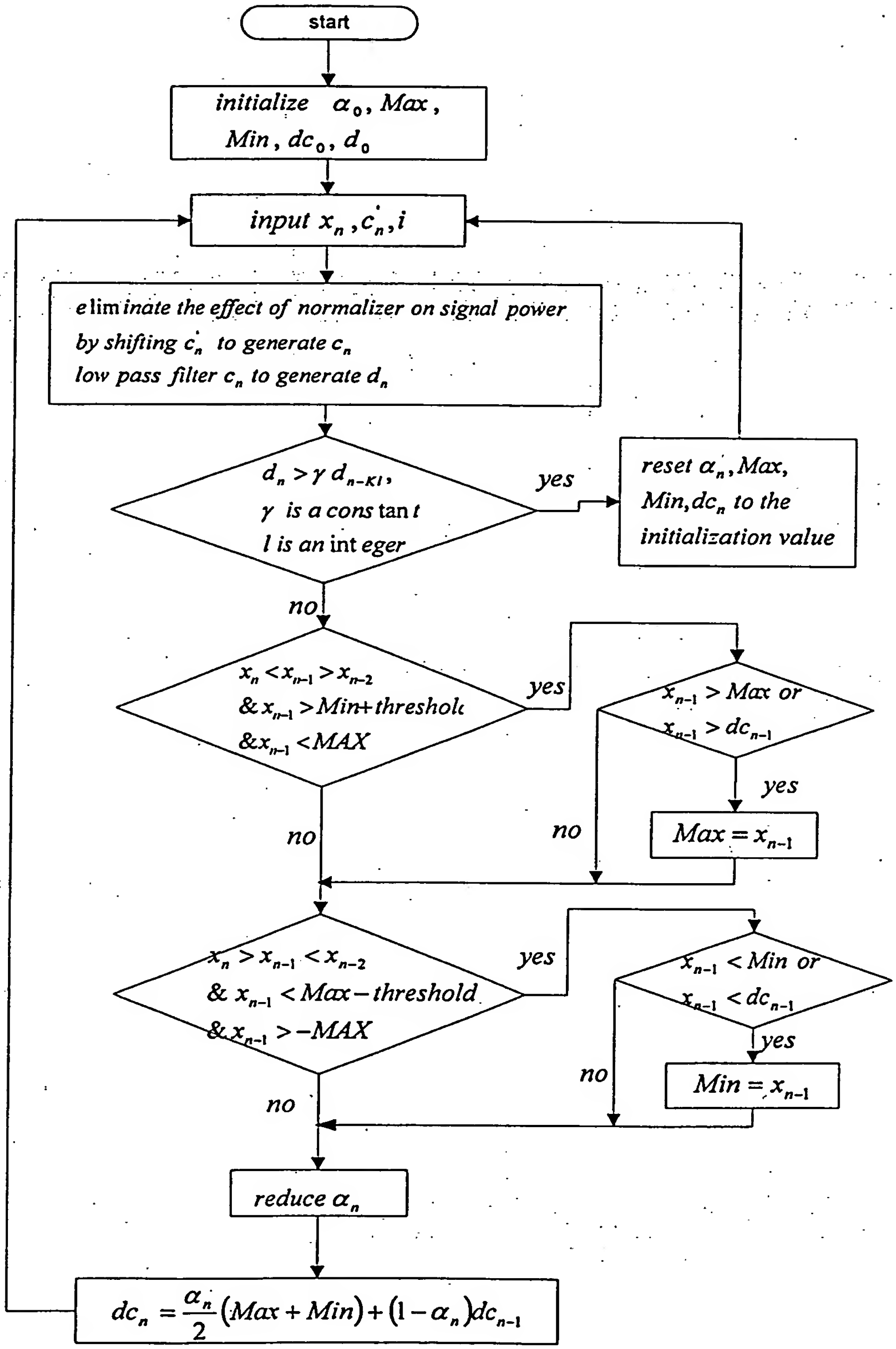
start
initialize α_0, Max, Min, dc_0, d_0
input x_n, c'_n, i
eliminate the effect of normalizer on signal power
by shifting c'_n to generate c_n
low pass filter c_n to generate d_n
$d_n > \gamma d_{n-Kl}$,
γ is a constant
l is an integer
yes
reset α_n, Max, Min, dc_n to the initialization value
no
$x_n < x_{n-1} > x_{n-2}$
$\& x_{n-1} >$ Min+threshold
$\& x_{n-1} < MAX$
yes
$x_{n-1} >$ Max or
$x_{n-1} > dc_{n-1}$
yes
$Max = x_{n-1}$
no
no
$x_n > x_{n-1} < x_{n-2}$
$\& x_{n-1} <$ Max − threshold
$\& x_{n-1} > -MAX$
yes
$x_{n-1} <$ Min or
$x_{n-1} < dc_{n-1}$
yes
$Min = x_{n-1}$
no
no
reduce α_n
$dc_n = \frac{\alpha_n}{2}(Max + Min) + (1 - \alpha_n)dc_{n-1}$

FIG. 10